

Understanding the Target Impedance Mask

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2020.3.12

Keysight Power Integrity Applications Expert

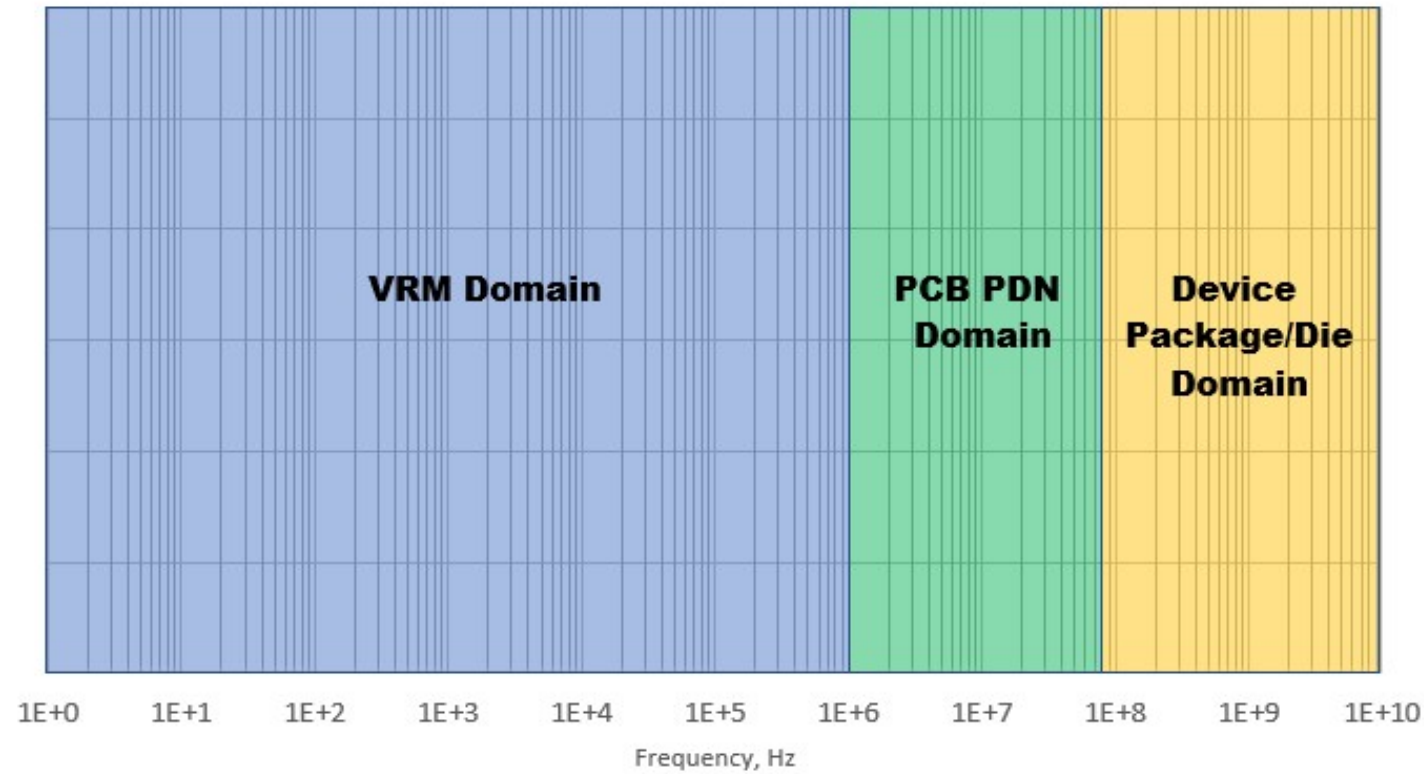


Topics

- **PDN Impedance Mask**
- **Powering High Speed 58Gb/s PAM4 SerDes**
- **Powering High Current FPGA Dynamic Loads ?**

PI Impedance Domains

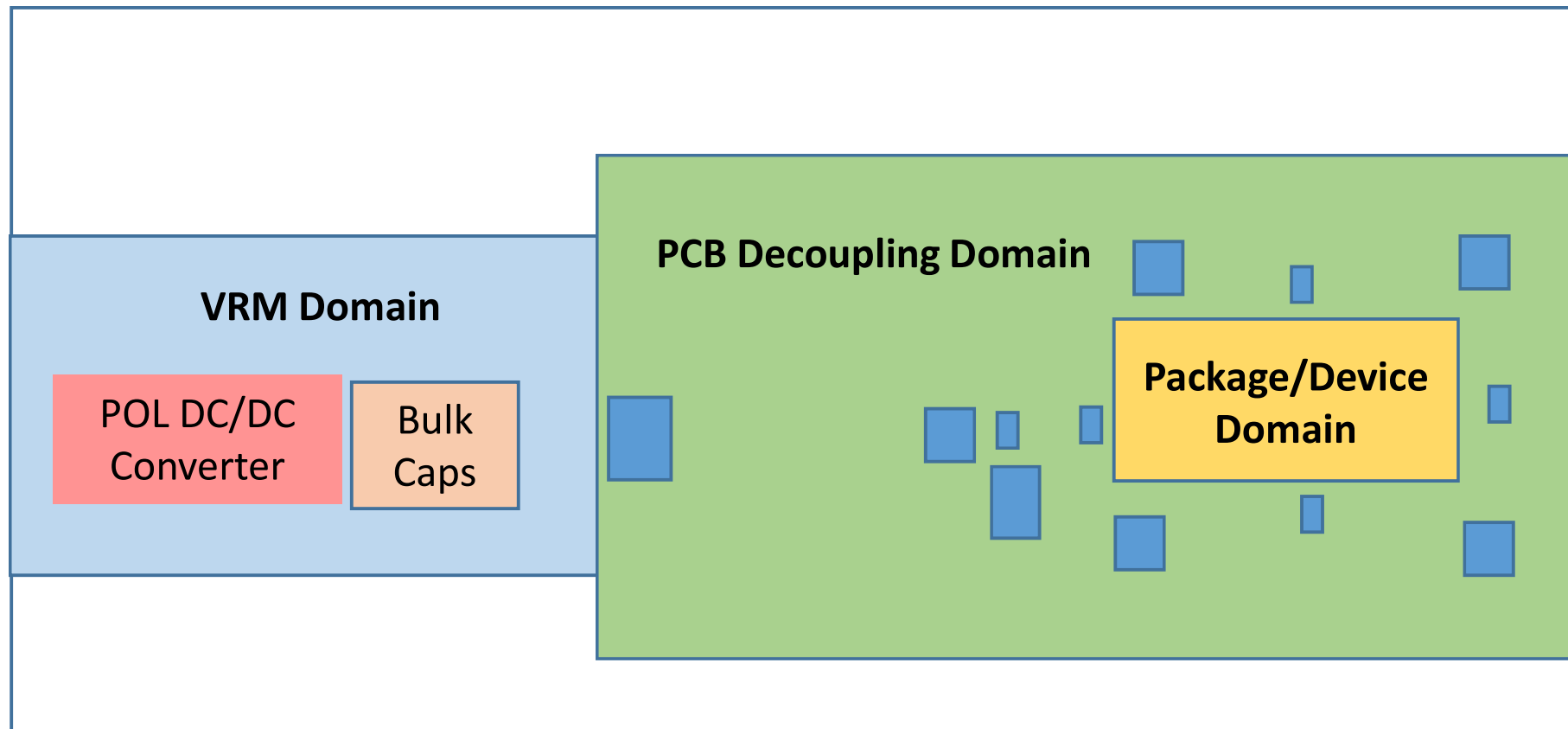
Regions of Impedance Control



regions of Power Supply impedance concern/control/effect

PI Spatial Impedance Domains

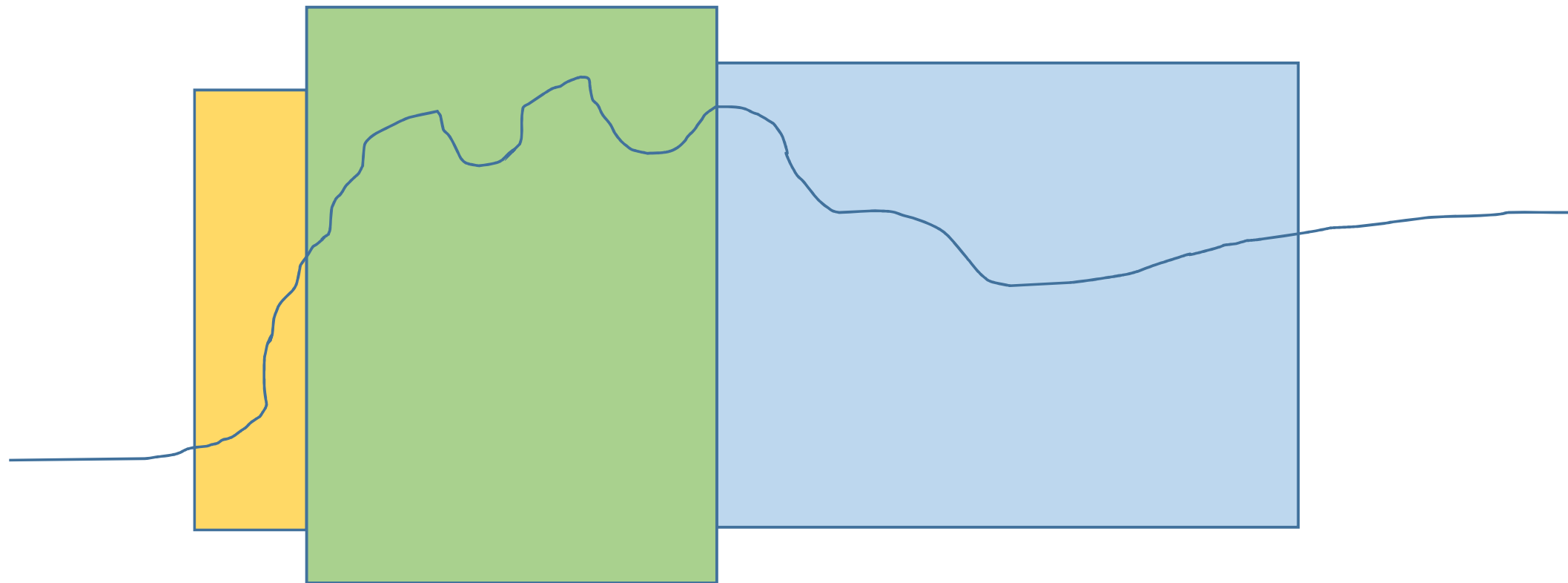
Keep dynamic current local, reduce PDN delivery as static as possible! If everything is DC then radiated is minimized... DC does not resonate.
Waterfall charge storage to minimize high current loops????
PI Impedance vs. Frequency relates to the spatial PI Domain!



Flip sideways to show current loops....limit the spatial di/dt to reduce coupling/conducted EMI?

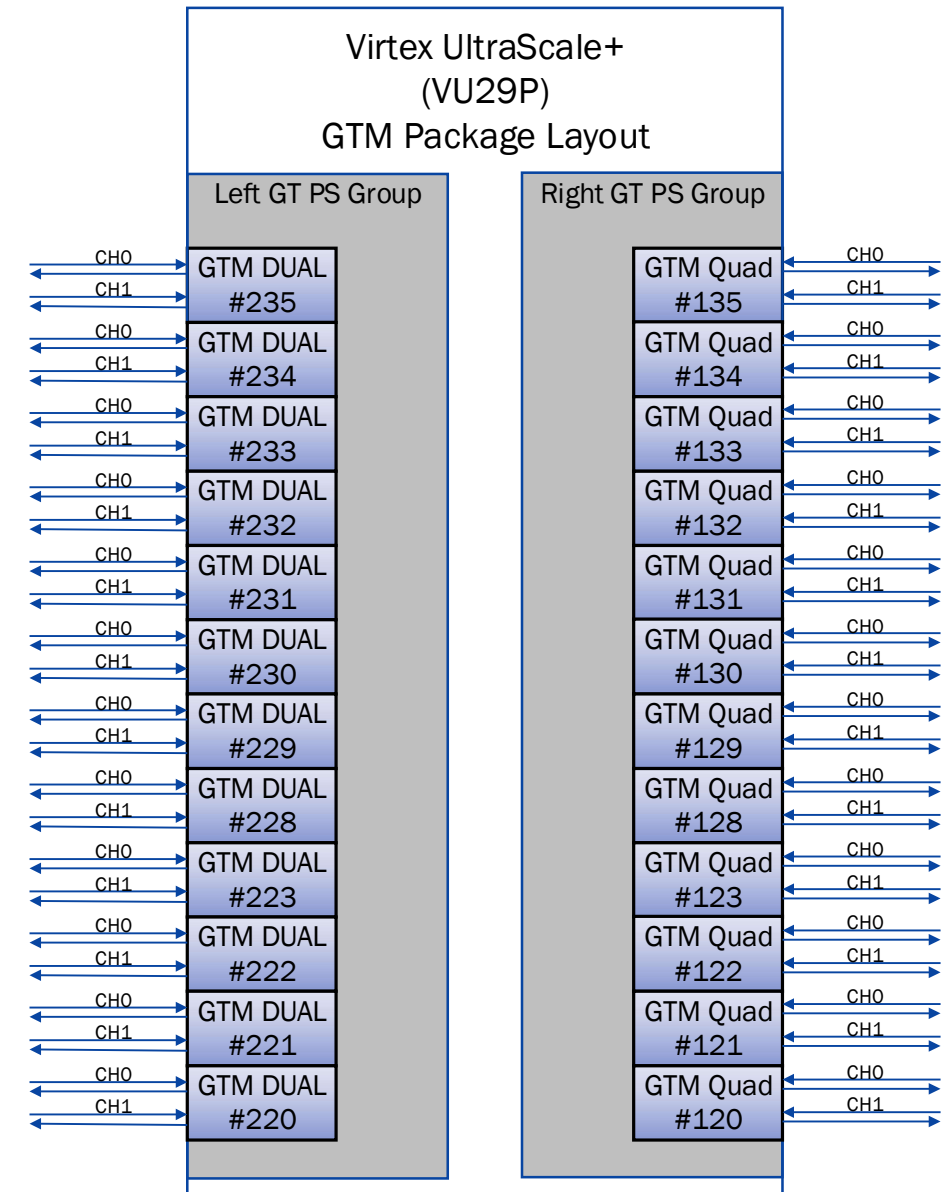
PI Domains in Time?

Step Load Response Debugging.....

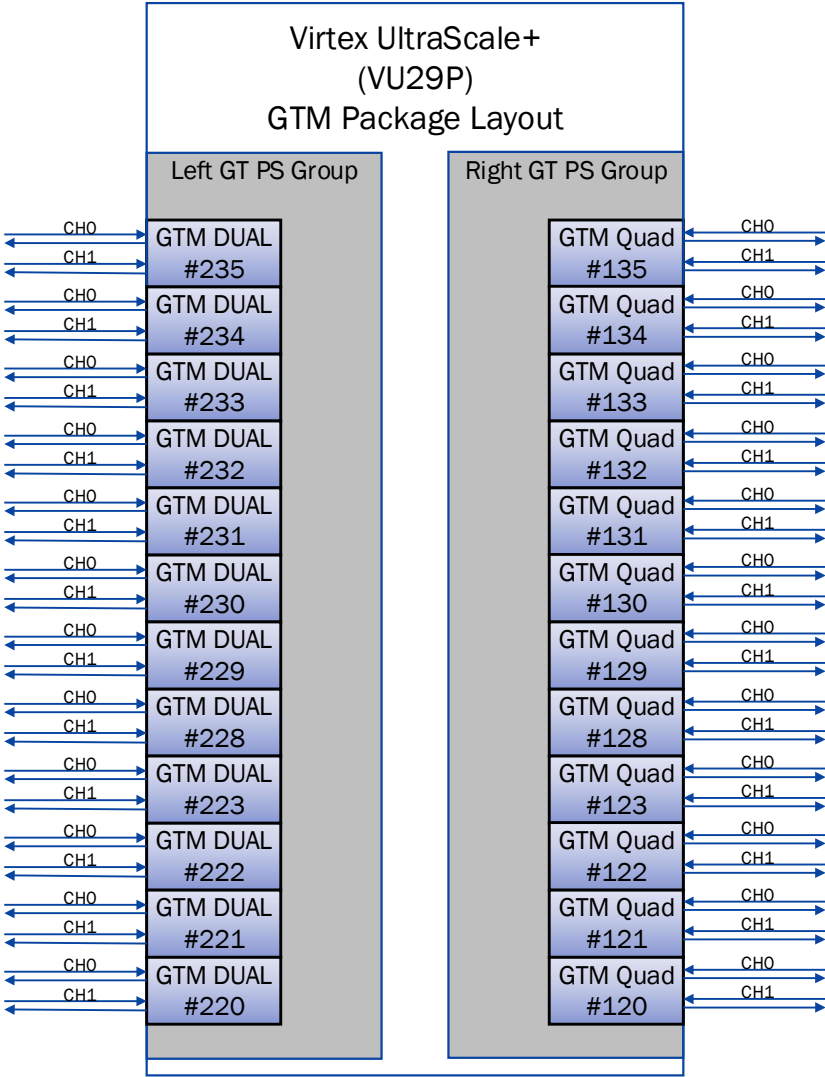
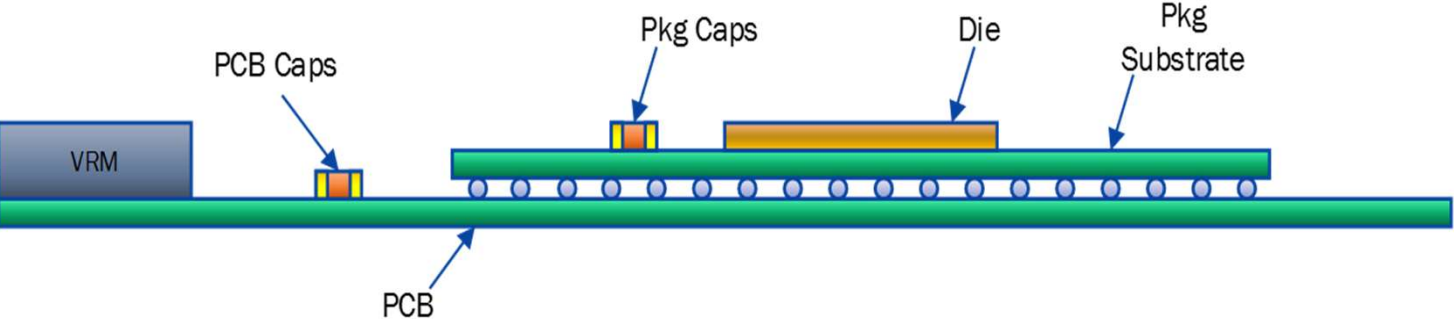
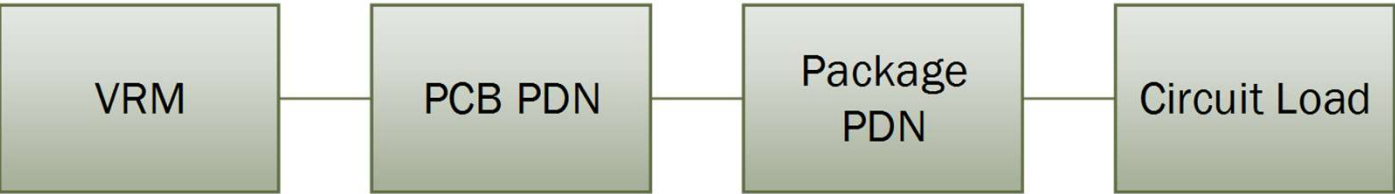


Powering 58Gb/s PAM4 SerDes

- UltraScale+
- XCVU29P-FSGA2577
- 58 Gbps PAM4 Transceivers, 48 ea
- Package: 52.5mm x 52.5mm, 2577 pins



58 Gb/s SERDES Power Integrity Ecosystem



58G SerDes Power Supplies

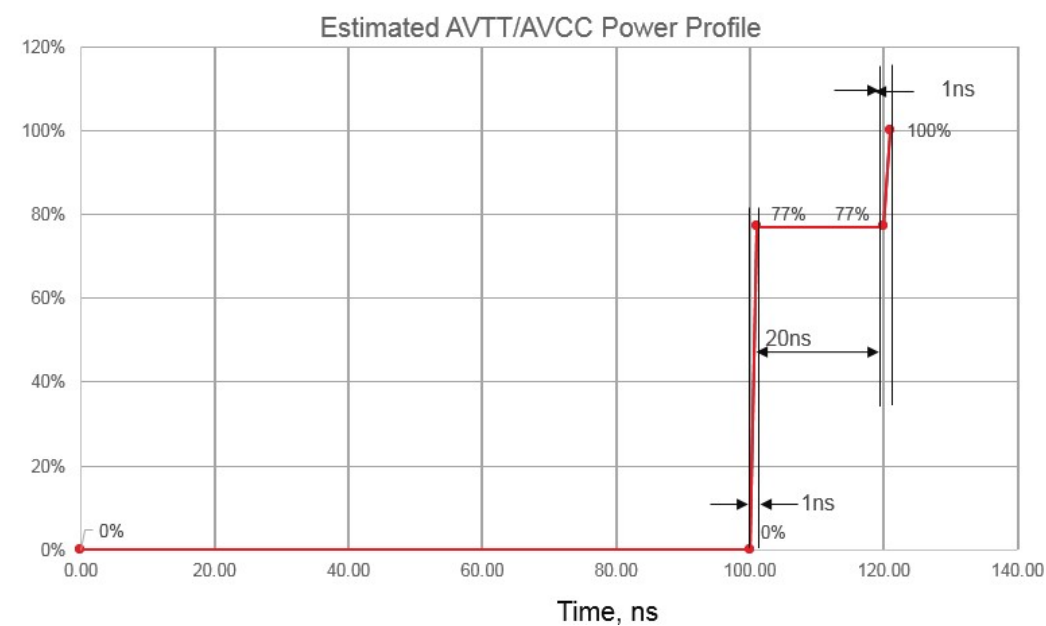
➤ Power Supply Voltages

- MGTMAVCC: 1.2V
- MGTMAVCC: 0.9V
- MGTMVCCAUX: 1.8V

➤ Types of Power Supply Stress

- Mission Mode Noise
- Crosstalk Noise
- System State Change Noise

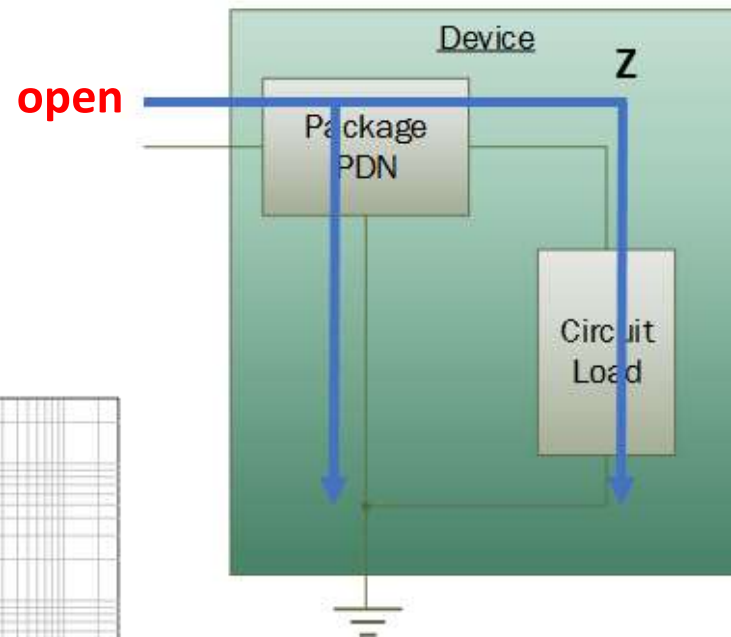
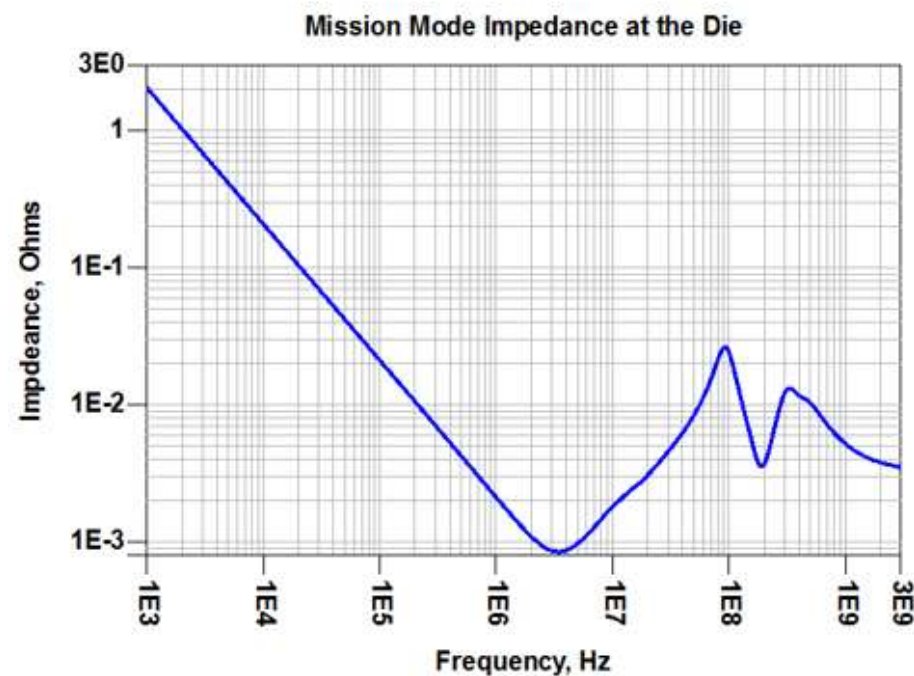
Power Rails for 58Gb/s PAM4 SerDes



Power Supply	Vnom (V)	Current per Dual (mA)	Total Current 12 Duals (mA)
MGTMAVCC	0.9	306	3672
MGTMAVTT	1.2	419	5028
MGTMVCCAUX	1.8	18	216

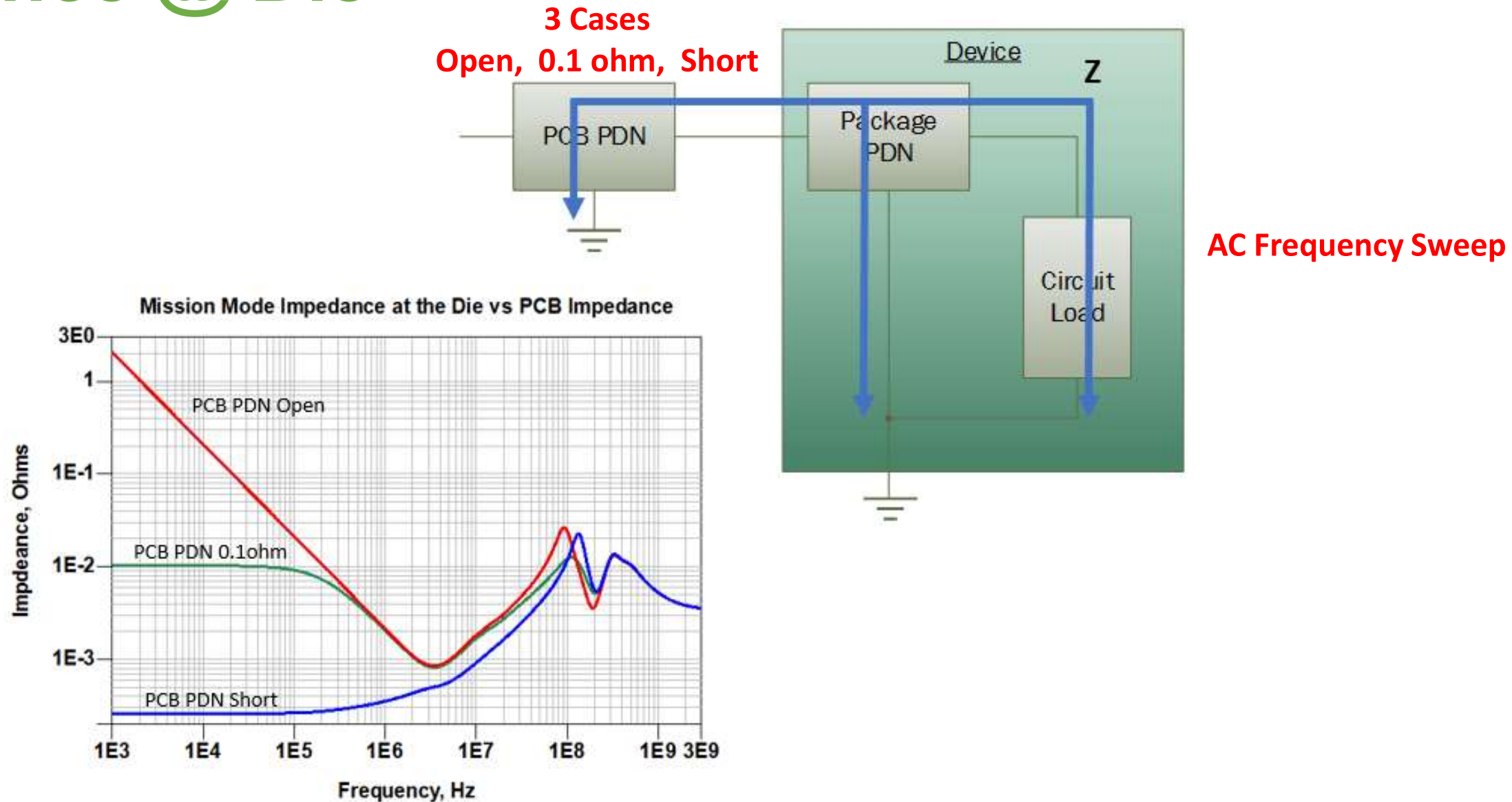
Note: Current calculated using *UltraScale_Plus_XPE_2018_3.xlsm* downloaded from www.xilinx.com.

Transceiver Package and Die Model



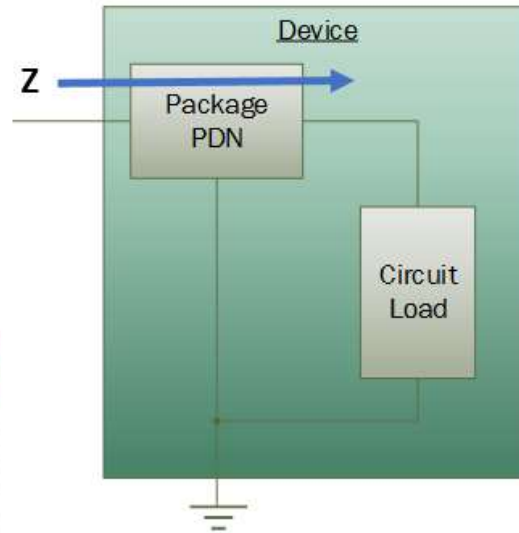
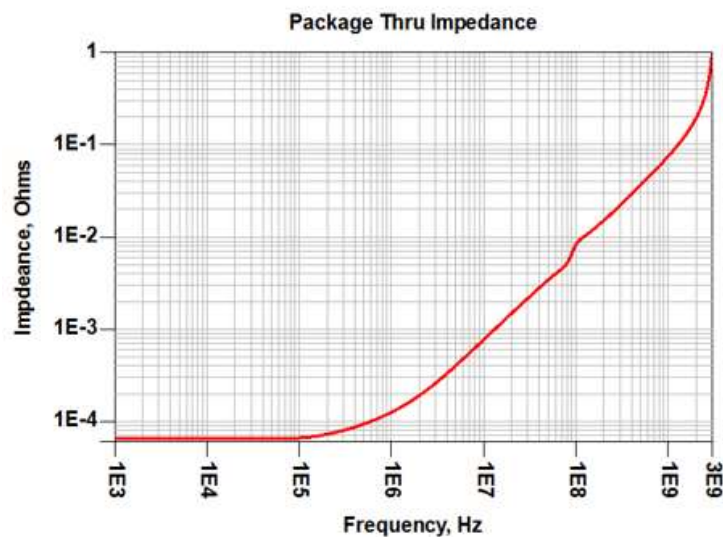
AC Frequency Sweep

Transceiver Package and Die Model Impedance @ Die

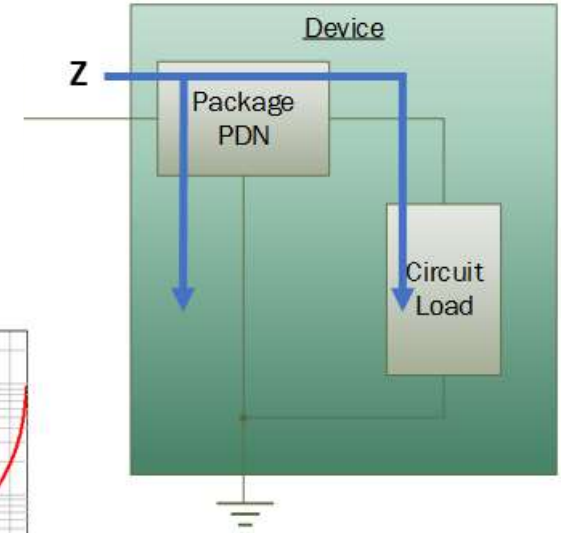
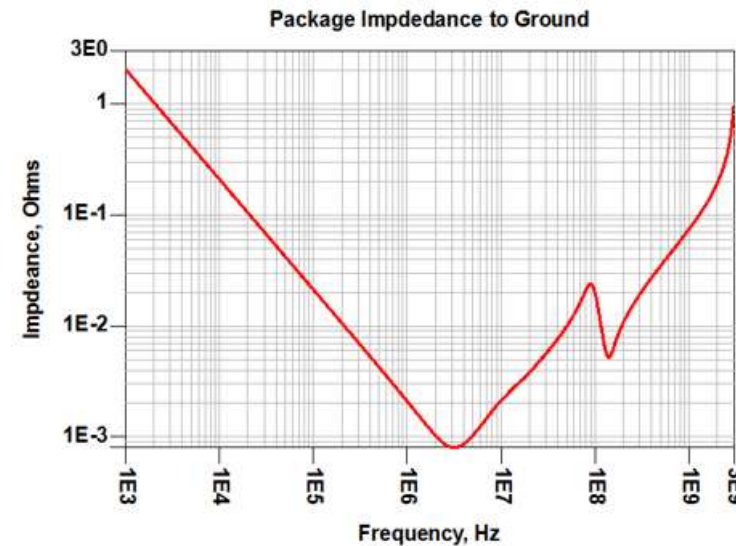


Transceiver Package and Die Model Impedance @ Package Pin

Transfer Impedance Package Pin to Die



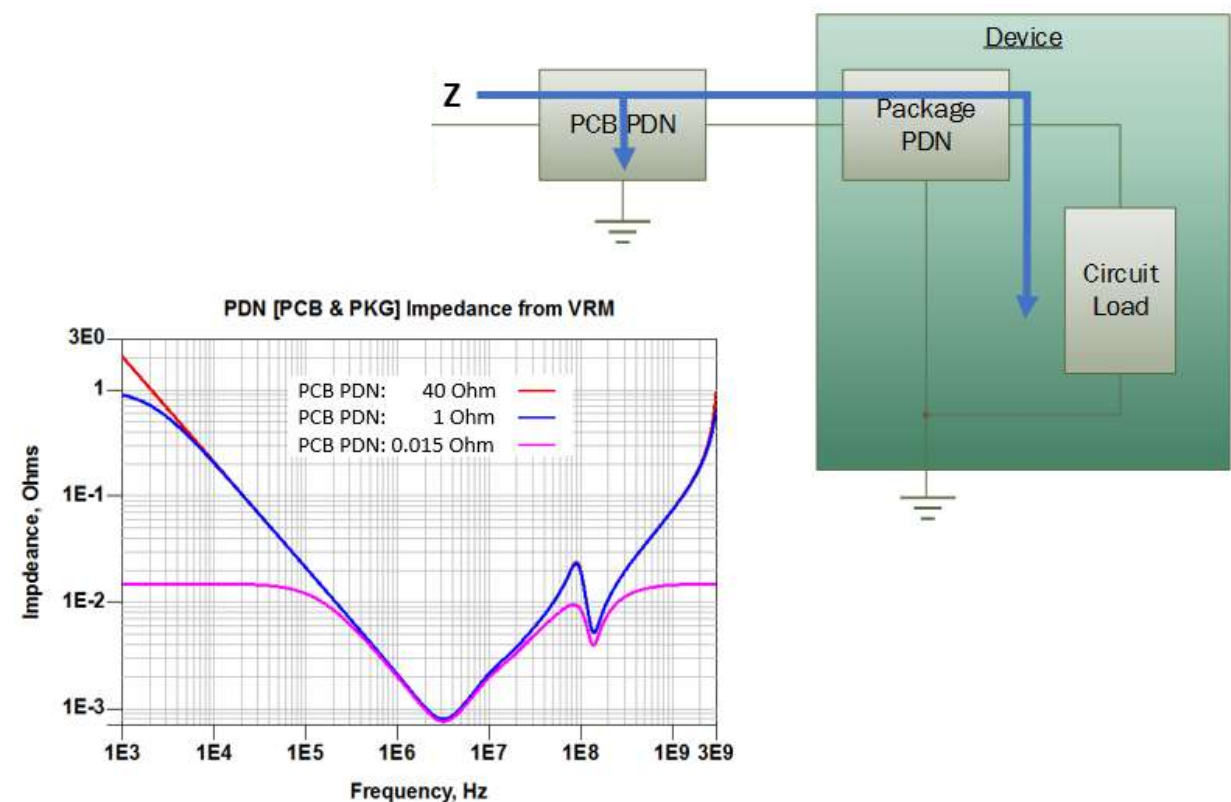
Impedance at Package Pin



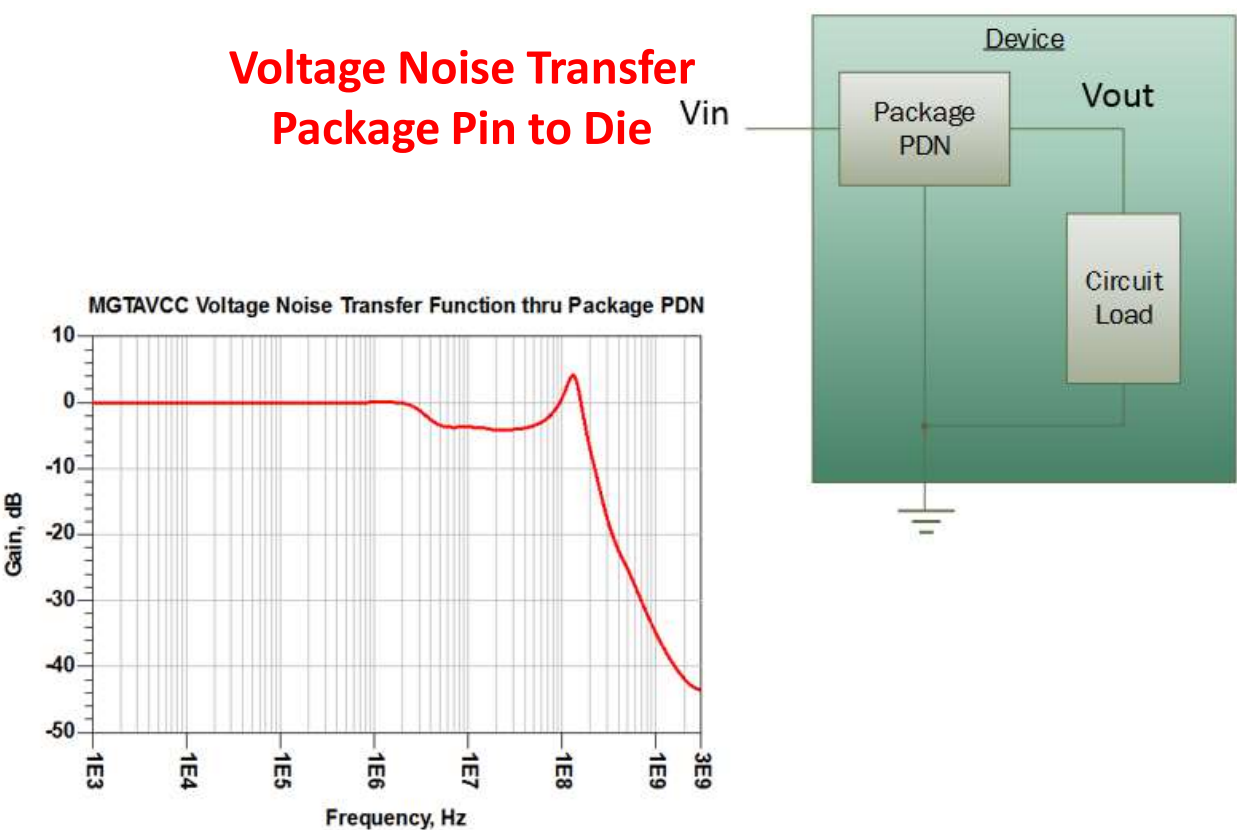
Transceiver Package and Die Model

Transfer impedance thru PCB and Package

Transfer Impedance PCB and Package Pin to Die

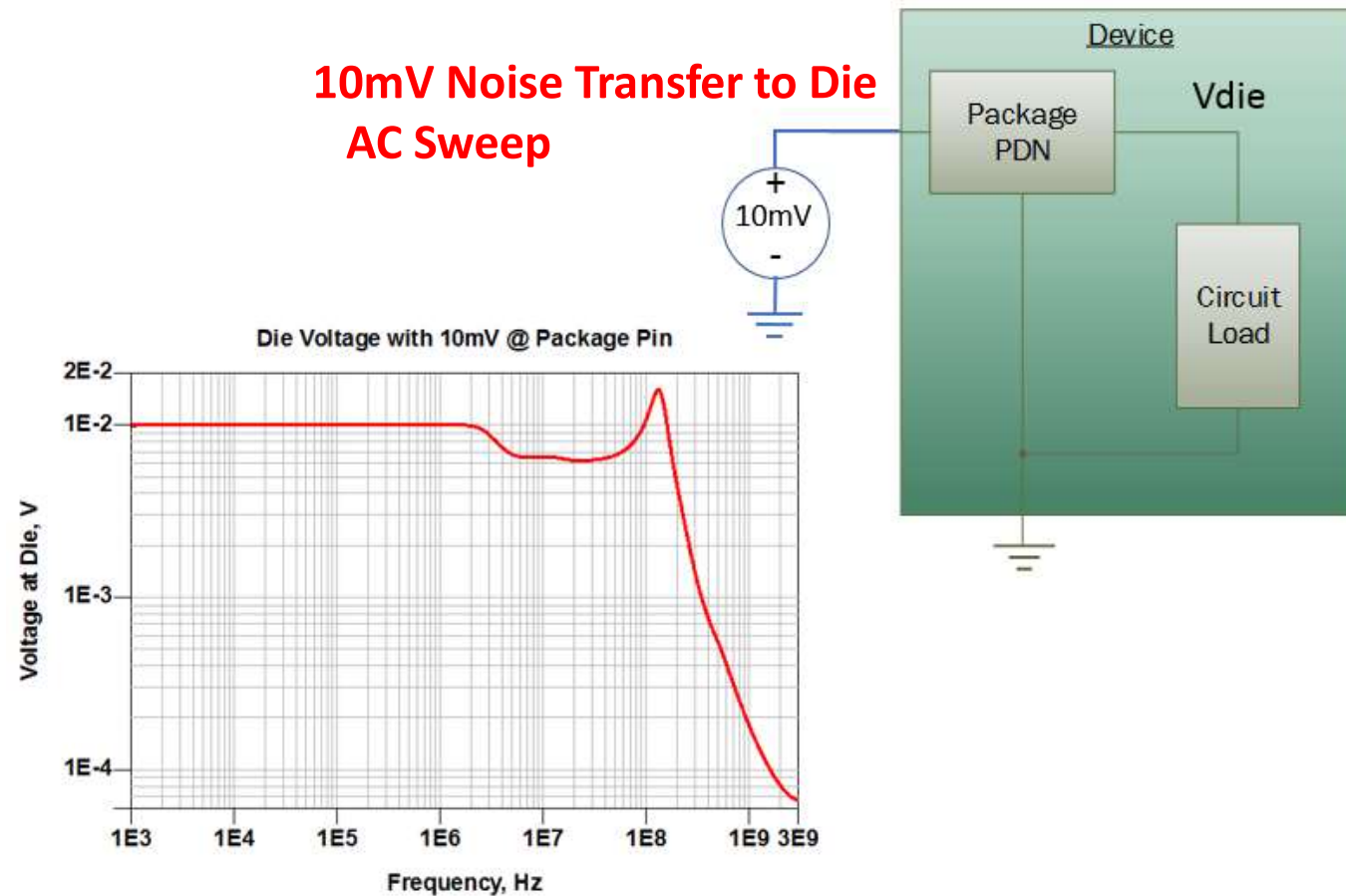


Voltage Noise Transfer Package Pin to Die



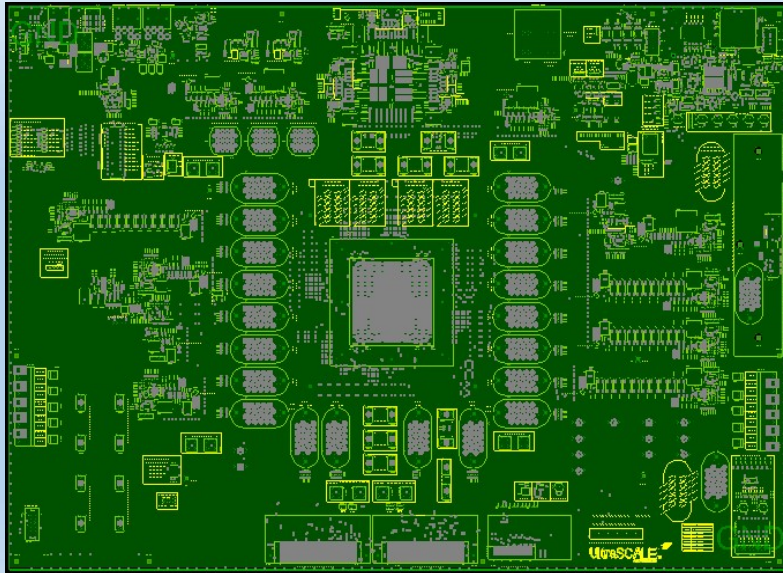
Transceiver Package and Die Model

Power Supply Voltage Transfer Function

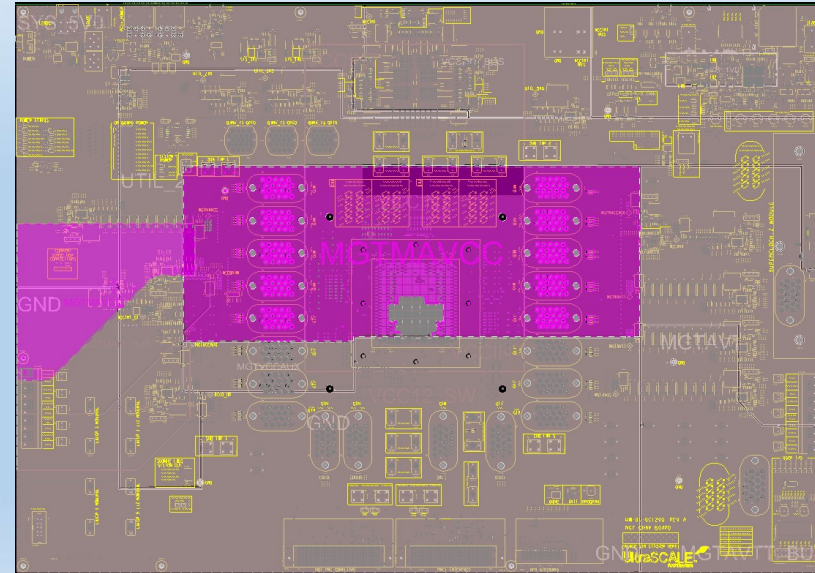


MGTMAVCC PCB Power Plane Layout

PCB Physical Layout



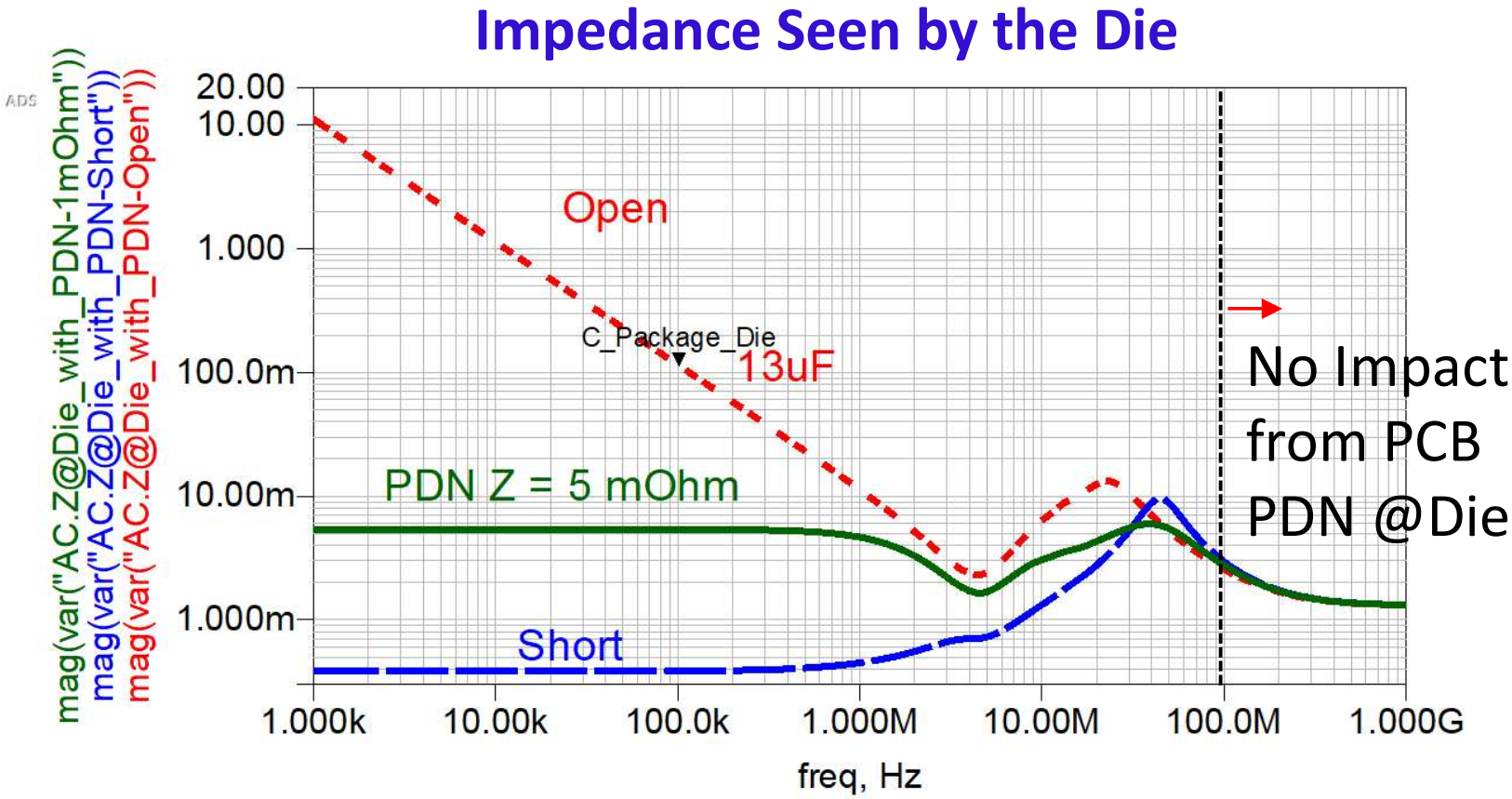
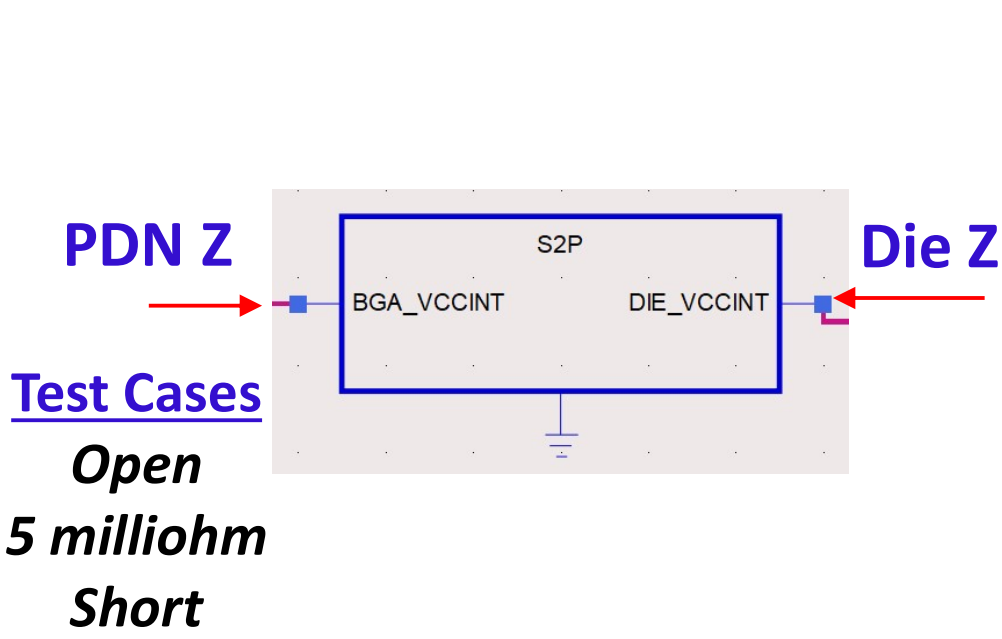
PCB MGTMAVCC Physical Layout



Topics

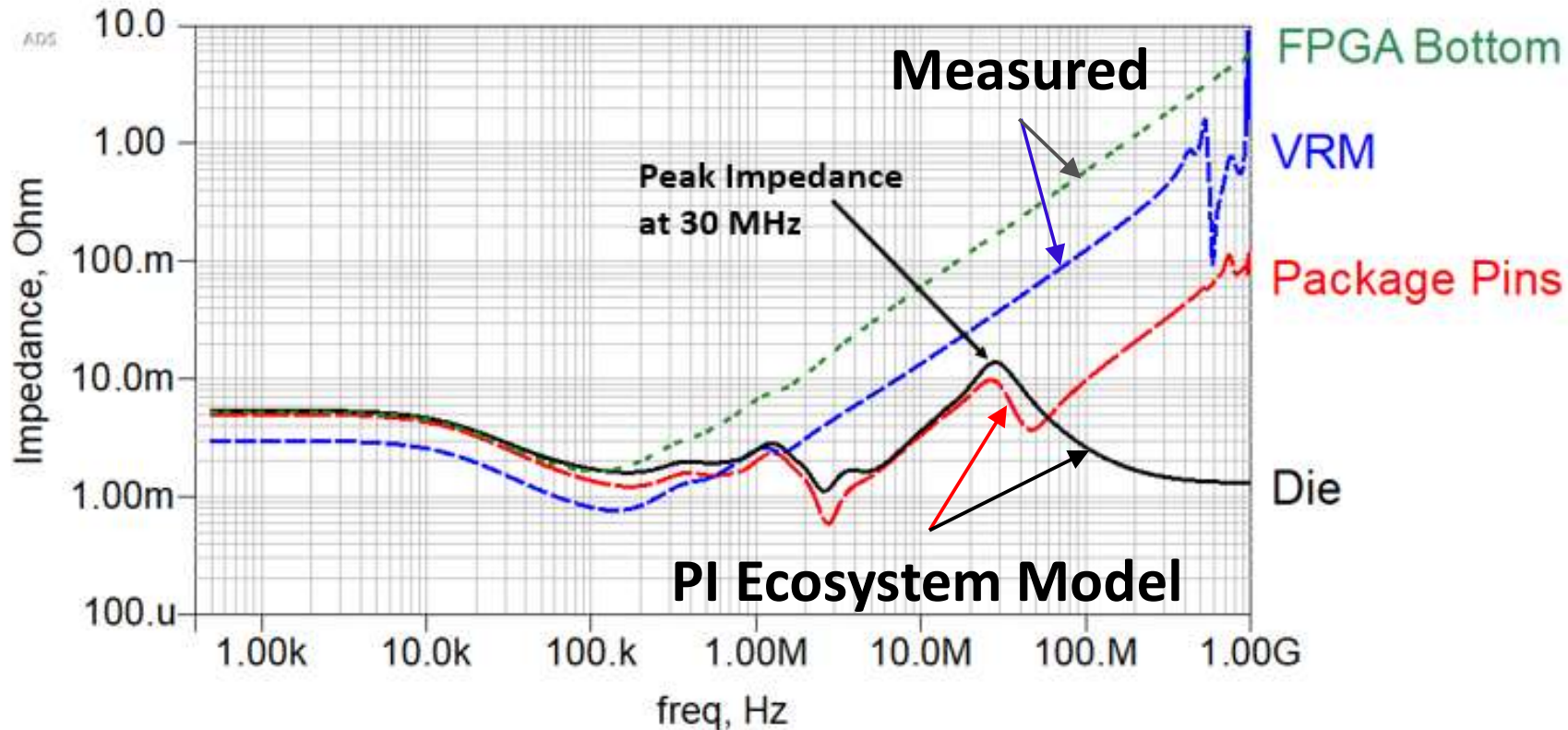
- **PDN Impedance Mask**
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- **Powering High Current FPGA Dynamic Load**

FPGA Package/Die Model for Main Supply VCCINT



FPGA and PCB Decoupling Capacitor Models are Critical

Impedance measurements did not see the resonance at 30 MHz!



- Decoupling capacitors dominate the impedance of the VCCINT PDN.
- Measurements with VCCINT are only accessible on the bottom side of the FPGA and include the via inductance.
- PIPro PDN EM model with package/die (CPM) in ADS schematic accurately predicts impedance peak that measurement could not see.

Summary

- SERDES Transceiver Mission Mode switching frequencies are handled by the package/die decoupling.
- Powering Transceiver's on/off for low power operation can result in much lower frequency power demands.
- Package/Die models provide Impedance vs. Frequency performance for understanding Target Z requirements.
- Step Load di/dt excites the PDN impedance to determine max ripple voltage.

Hands-On Lab 2:

200128_PI_Lab2_Load_wrk.7zads

Basics – Instructor Led Demo

Transceiver Turn-on with ideal R-L PCB PDN

Frequency Domain Impedance and Time Domain Excitation for ripple

Explore –

Package Model Impedance

Impedance at Package Pin vs. Die

Advanced –

Tune C_{total} for a given Target Z profile

Thank You!

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Questions?